1980

Automatic, Remote Status Lights for VAX UNIX

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ABSTRACT

The Computer Science Department's VAX 11/780 runs unattended four floors below the users. In order to communicate the system status to users, automatic status lights were designed and installed. This report documents the simple device that controls the lights, and the UNIX processes used to signal it.

1. Introduction:

The Computer Science Department at Purdue University owns and operates a Digital Equipment Corporation VAX 11/780 computer. The machine is physically located four floors below the Departmental offices and terminal rooms, and normally runs unattended. Users, as well as student operators, need to know 1) whether problems they encounter are due to the system or their individual programs/terminals, 2) whether an operator is attending to a system crash, and 3) how long the machine will be out of service. Finally, a few users schedule machine time for non-UNIX systems, or for work that prohibits normal operation. To inform users of the system status, a set of automatic status lights have been designed and installed. This report documents the design and hardware, and describes the operation of the UNIX processes that support it.

2. Early Design:

The original plan was to build as simple a device as possible. The constraints were:

1. Spend as little time and money as possible.
2. Use no more than 4 wires to connect the machine room to the user area (4 wires were available in an existing cable). Moreover, the wires could not handle more than a few milliamps of current.
3. Use a pair of lights on hand that had one red, and one green light.

Meanings were assigned to the lights as follows:

Red	Green	Meaning
off	off	no information
on	flashing	coming up soon
off	on	UNIX up
flashing	on	going down soon
on	off	system down
off	flashing	non-UNIX system up

Table 1. Interpretations for the lights.

The hardware to support the status lights was designed as shown in Figure 1. The logic and power supply resided in one unit that was kept near the status lights. A remote unit, located in the machine room, used red and green LED indicators in place of lamps, so it required very little current. Of the four wires connecting the control unit to the remote unit, two carried the red and green signals, the third went to a SPST pushbutton switch, and the fourth served as a common ground. The control unit included an identical pushbutton switch wired in parallel.

To select a configuration, one merely pressed either switch repeatedly until the desired state was reached; there was no connection to the computer. This manually operated version of the lights was built, but while waiting for the lights to be installed, we began toying with the possibility of connecting the control unit to the machine in order to change the state automatically. Although several different connection schemes were considered, our final choice was biased by the existing control unit, and a desire to avoid modifying the VAX hardware.

3. Final Design:

In order to connect the control unit to the computer, it had to be located in the machine room. Unfortunately, the control unit had been designed for use in the user area, and the small gauge wire from the machine room to the user area could not carry enough current to power the lamps. Plans were made to swap the control and remote units, and a power supply was installed in the remote unit as shown in Figure 2. Sensitive relays that required very little current were used in the remote unit to switch the lamps (the available solid state switches required at least 13 ma and had a high internal resistance, while the relays required only 6 ma).

Meanwhile, the circuit was modified by adding an interface to the VAX. The interface was connected to the VAX through an asynchronous RS232 terminal port on the UNIBUS. In order to fit everything into the existing chassis, we chose not to decode the incomming signal with a UAR/T, but rather to time successive signals. Of course, adding this part of the circuit after the original pieces were implemented meant using spare gates whenever possible.

4. Circuit Operation:

The circuit, shown in Appendix 1, should be considered in two parts. The first part consists of the 74121 debouncer (monostable multivibrator), 7493 counter, and 7442 decoder; it is the heart of the manual state selector. Pulses from pushbutton switches connected to point B are squared by the debouncer and fed to the counter. Normally the counter is enabled for counting, and counts the pulses, sending the result (in binary) to the decoder. The decoder, in turn, selects exactly one of its output lines to be low corresponding to the count presented to its input. When the count reaches 6, pin 7 of the decoder is driven low and resets the counter through an inverter. To the user, it looks as if the 6 valid states are arranged cyclically with the "no information" state immediately following the "alternate system" state (refer to Table 1 for the interpretations of states).

The lights are switched by reed relays which are, in turn, driven by 2N4400 transistors tied to the outputs of 7420 NAND gates. Decoder output lines that pass directly to the 7420 force the light *ON* when they are selected. For those states that require flashing, a 555 timer is set up to provide a square wave pulsing roughly once per second. Decoder output lines that correspond to flashing states are ORed with the timer pulse, using a 7402/7404 pair, before being passed to the 7420.

The second part of the circuit monitors system status. Standard RS232 signals from an asynchronous port enter the circuit at point A in the schematic, and are converted to TTL levels by the 1489 line receiver. Whenever UNIX is up, it sends a character out every two seconds. When the character is received, the line leaving the 1489 drops (perhaps more than once) and then returns high. The 1489 output connects to the reset on a 7493 counter through the 7400 NAND gate, and into a 7402 NOR gate. The 7400 is enabled whenever one of "UNIX up" or "going down soon" states has been selected, and passes the reset signals through; the counter remains reset in the other four states. If the counter reaches a count of 8, it will toggle the 74121 just like a pushbutton. Therefore, the heart of the detector is a simple 8-second counter that is enabled whenever UNIX is running, and reset whenever UNIX sends a character out the port. If 8 seconds goes by before another character is received, the lights change from "UNIX up" to "going down".

The remaining gates, 2 NANDS, a NOR, and 2 inverters add one fancy touch. They monitor the "coming up soon" state and connect the 1489 receiver output

to the 74121 debouncer when "coming up" has been selected. In any other state, they feed the high order bit of the 7493 counter output to the debouncer as described above. Thus, when the state is set to "coming up", any output from the system will toggle the lights into the "UNIX up" state.

5. Bugs in this design:

The only know bug in the circuit actually turns out to be an advantage. When the timer pulses 8 times without a reset signal, the high order bit of the 7493 comes on and togglesthe state of the lights from "UNIX up" to "going down" as described above. The counter is not reset, however, so it continues to count while holding the bit high. This disables the debouncer so it ignores manual signals for a short time. Finally the counter reaches 15 and when the next pulse is received, it resets to 0 and the high order bit drops. Another 8 seconds passes before the count reaches 16 and the state changes again. Thus, there is a 16 second "window" in which UNIX can reset the counter. In order to change the lights from "UNIX up" to "going down" UNIX must stop sending characters for between 9 and 23 seconds. In a time-shared environment where exacty delays are difficult to produce, this wide window is an advantage.

6. UNIX Processes and Status Lights:

The UNIX process to send a character to the status light control unit is shown in Appendix 2. Bascially, it consists of an infinite loop that sends out a single character every 2 seconds. When it begins, the process writes its id on file "*/tmp/lightid*" so the system shutdown process will be able to signal it.

Authorizied users can shutdown UNIX with the command *zzz*. At 10 minutes to shutdown, *zzz* executes file "*/etc/ec.10*". Located in this file is the command:

kill -2 'cat */tmp/lightid*'

which reads the process id of the status lights, and then sends it signal 2. Upon receiving the signal, the status light process suspends itself for approximately 10 seconds and then resumes output. During the pause, the lights change from the "UNIX up" state to the "going down" state, and remain that way until system shutdown. As mentioned above, the timing is not critical, any delay between 9 and 23 seconds will suffice.

To start the status lights, an operator manually selects the "coming up" state and boots UNIX. After checking for file system errors, the operator leaves single user mode and the system executes file */etc/rc* to bring up the multiuser system. */etc/rc* executes file */etc/Lights* which forks off and runs in the background as long as UNIX is up. The first character sent to the control unit changes its mode from "coming up" to "UNIX up". From an operator's viewpoint the sequence of states "coming up" "UNIX up", "going down", and "system down" is completely automated.

7. Future Plans:

We are basically happy with the status lights. On occasion, however, UNIX gets so loaded that the process driving them cannot respond within 8 seconds. At first we thought about arranging to change back into the "UNIX up" state automatically when characters began arriving again. Doing so would eliminate our ability to automatically switch into the "going down" state during scheduled shutdown, so the idea was abandoned, at least for the present.

A more sophisticated set of status lights seems to require far more sophisticated hardware. For one thing, characters should be decoded as the come from

the machine to enable UNIX to give a more precise indication of the desired state. Because the number of gates required for a combinatorial circuit would be large, a microprocessor might be more effective. Since the Department has acquired a PDP 11/40 for use as a front-end machine, it might be possible to use it to write messages directly to users' terminals, providing even better status information than the lights.

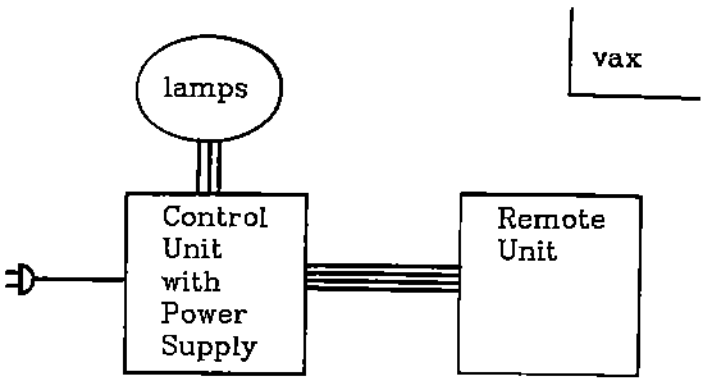


Figure 1. The original hardware configuration.

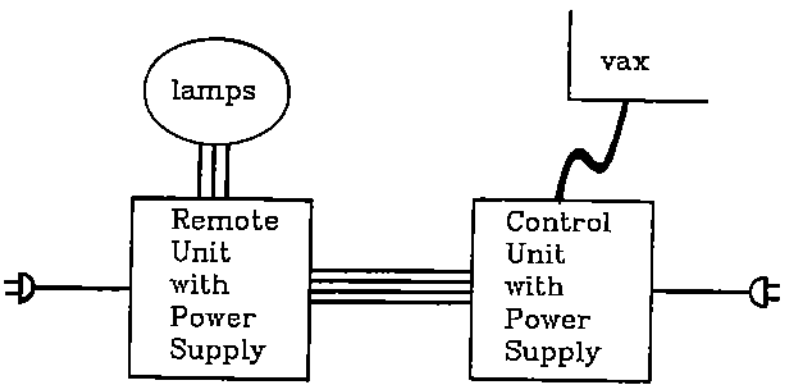
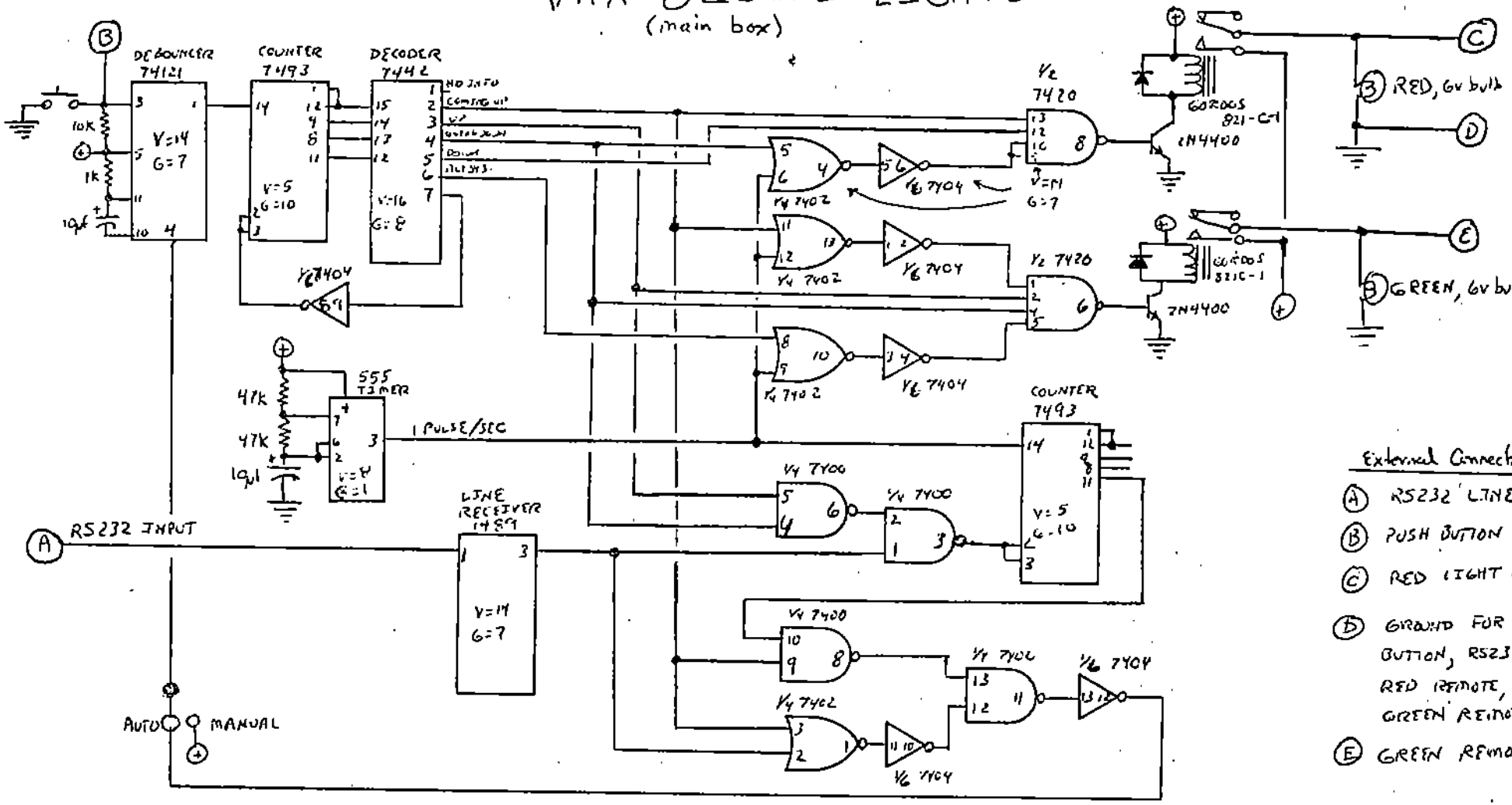
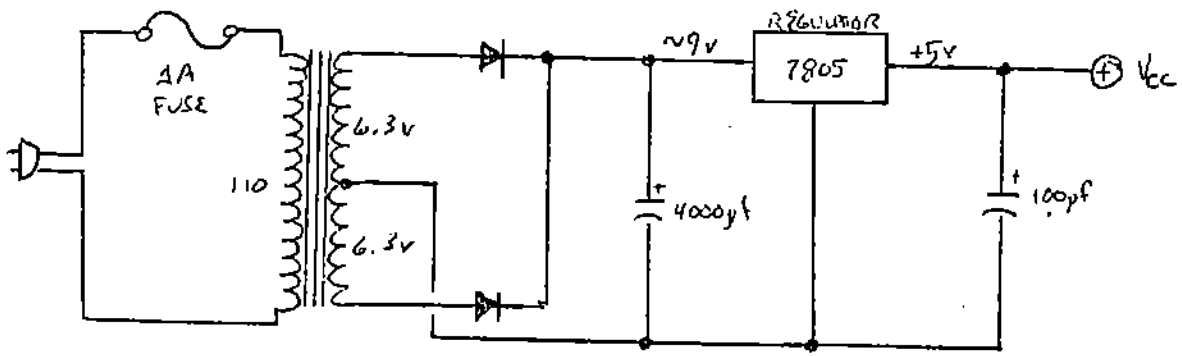


Figure 2. The final hardware configuration.

VAX SIGNAL LIGHTS
(main box)





External Connections

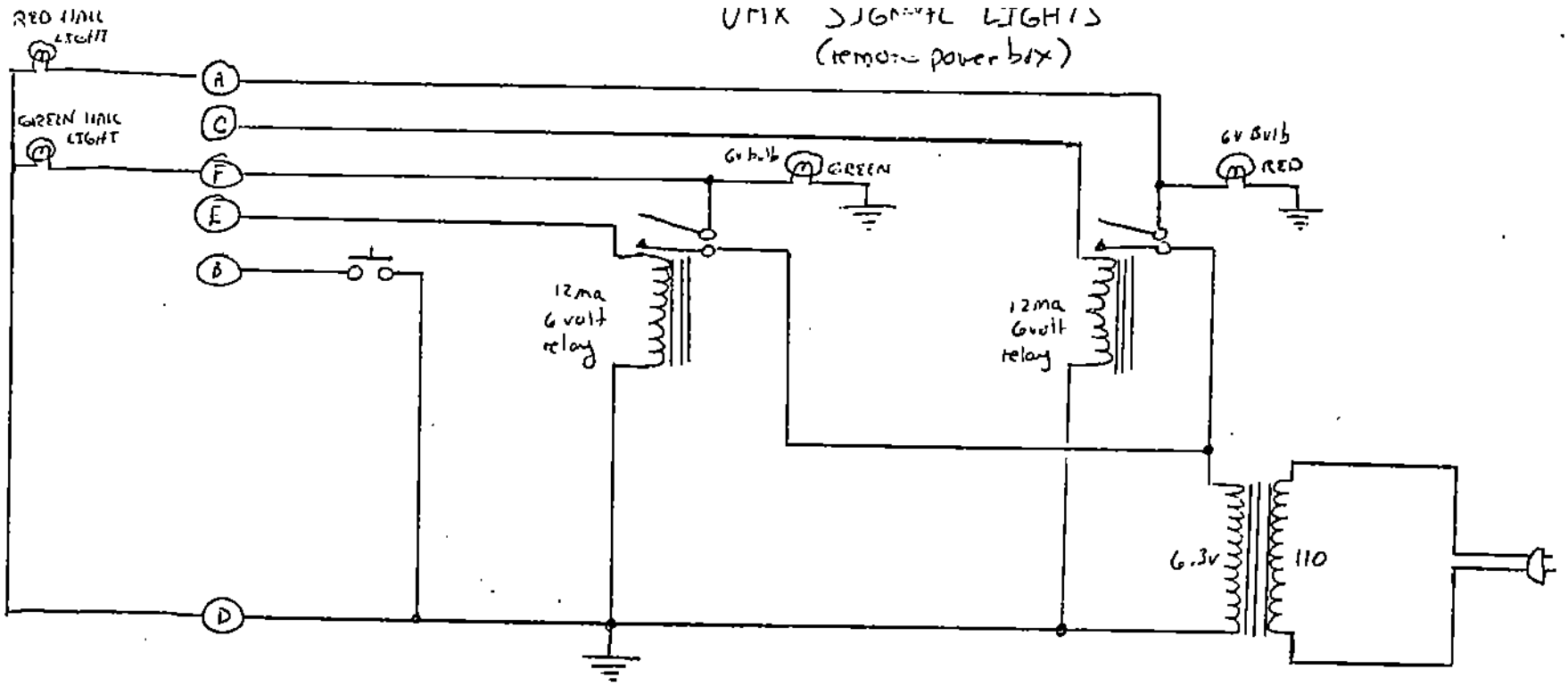
- (A) RS232 LINE (PIN
- (B) PUSH BUTTON
- (C) RED LIGHT REMOTE
- (D) GROUND FOR PUSH-BUTTON, RS232 LINE, RED REMOTE, and GREEN REMOTE
- (E) GREEN REMOTE

STATE (COUNT)	7442 PIN	RED	GREEN	MEANING
0	1	0	0	No Info
* 1	2	1	F	UNIX coming up
* 2	3	0	1	UNIX up
* 3	4	F	1	UNIX going down
4	5	1	0	Down
5	6	0	F	Alternate system up
6	7	–	–	Reset to state 0

*toggles out of this state automatically

dec & rlb
3/81
1 of 2

UNIX DIGITAL LIGHTS
(remote power box)



External Connections

- (A) To Red hall lights
- (B) From (B) on main box
- (C) From (C) on main box
- (D) From (D) on main box (also ground for hall lights)
- (E) From (E) on main box
- (F) To Green hall lights

Wire color codes

id	main box to cable	cable to 4th	cable to remote box	to hall lights	comes
(B)	WHITE	RED	WHITE	—	Button
(C)	RED	Red (pair 77)	BROWN	—	Red remote
(D)	BLACK	ORANGE+WT (pair 77)	BLACK	BLACK	ground
(E)	GREEN	GREEN+WT (pair 54)	ORANGE	—	green remote
(A)	—		RED	RED	red hall lights
(F)	—		GREEN	GREEN	green hall lights
*(A)	RED (TO MX)				RS232 from tty

*for main box only

Appendix 2

UNIX Status Light Signal Process

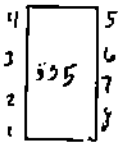
```
/*
 * Lights.c – Send a character to the lights every two seconds
 */
#include <signal.h>
#define  Boolean  int
#define  CHRLEN  1     /* character length for write */
#define  FALSE    0
#define  LIGHTS   "/dev/lights"
#define  OUTCHR  "A"  /* character to output to lights */
#define  PIDFILE  "/tmp/lightid"
#define  TRUE     1
#define  WRITE    1     /* write access for open */

Boolean hold = FALSE;
charcpid[6];              /* process id in ASCII */
int  i;
int  pid;                 /* this process's id */
int  fd;                  /* file descriptor */

/**********/
/*
/* godown – reached when 10 second delay is desired.
/*
/**********/
godown()
{
     signal(SIGINT, godown);
     hold = TRUE;
}
/**********/
/*
/* lights - output character to lights every second
/*
/**********/
main()
{
     if (fork()!=0) exit(0);
     signal(SIGQUIT, SIG_IGN);
     signal(SIGINT, godown);
     signal(SIGHUP, SIG_IGN);
     for ( i=0 ; i<3 ; i++ )
          close(i);
     fd = creat(PIDFILE, 0600);
     pid = getpid();
     for (i=0 ; pid ; ) {
          cpid[i++] = pid % 10 + '0';
          pid /= 10;
```

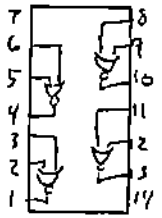
```
        }
    while (i)
        write(fd, &cpid[--i], CHRLEN);
    close(fd);

    fd = open(LIGHTS, WRITE);
    while ( TRUE ) {
        write(fd, OUTCHR, CHRLEN);
        if (hold) {
            hold = FALSE;
            sleep(10);
            }
        else
            sleep(2);
    }
}
```

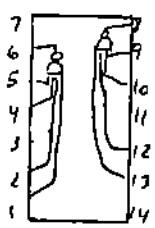
Appendix 3

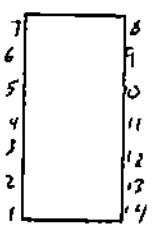
Physical Layout and Spec Sheets

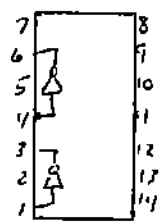
BOTTOM

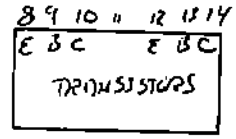


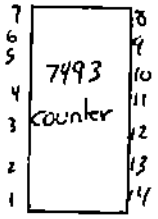


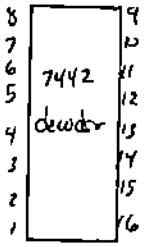


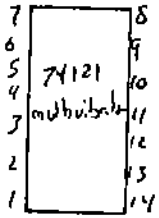


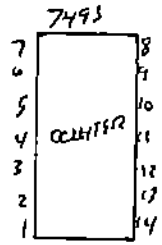


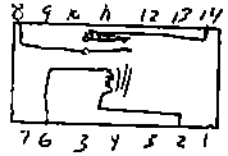












chip	page
7402	62
7409	63
7420	66
7442	167
7493	224
74121	82, 134
555	SIGNETICS
1489	3-5 INT. SEC.

2.5 Note that EIA standard RS-232-C is applicable only to the interconnection of DTE to DCE. It does not allow for the direct connection of two pieces of DTE; such as the direct connection of a terminal to a computer. Nevertheless, by making minor modifications to the RS-232-C rules, this can be accomplished, and frequently is. The procedure for doing this will be explained later.

3.0 Signal Levels

3.1 Positive RS-232-C signal levels are defined as a voltage between the range of +3 and +25 V.D.C. Negative signal levels are defined as a voltage level between the range of -3 and -25 V.D.C. The range between -3 and +3 V.D.C. is defined as the transition region. The signal state is not uniquely defined for this region.

3.2 Data signals are said to be in the "Marking" or "One" state when the signal level is negative. Data signals are said to be in the "Spacing" or "Zero" state when the signal level is positive.

3.3 Control and timing signals are said to be "ON" when the signal level is positive and "OFF" when the signal level is negative.

4.0 Pin Assignments

Although no signal connector is specified, the DB-25 is a widely accepted standard connector for RS-232-C.

4.1 For most applications, the important connector pin assignments are as follows:

Pin Number	Description
1	Protective (case) Ground
→ 2	Transmitted Data
3	Received Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
→ 7	Signal Ground
8	Received Line Signal Detector (Carrier Detect)
20	Data Terminal Ready

4.2 Pin 1 - Protective Ground. This pin normally need not be used if all equipment is properly grounded to a common point.

4.3 Pin 2 - Transmitted Data. This is the data path from DTE to DCE. In the case of a terminal, it is the data sent when something is typed at the keyboard.

4.4 Pin 3 - Received Data. This is the data path from DCE to DTE. In the case of a terminal, it is the data which is received by the terminal to be printed.

EIA interface to UNIX

NATIONAL

Line Drivers/Receivers

DS1488 quad line driver

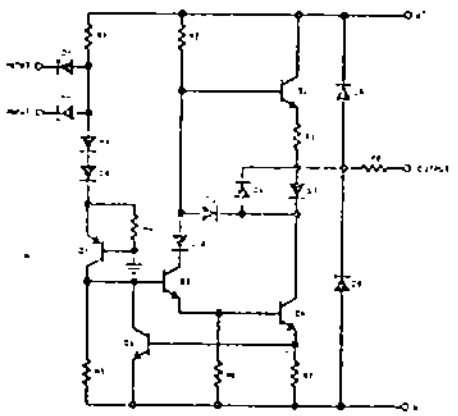
general description

The DS1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS 232C and CCITT Recommendation V. 24.

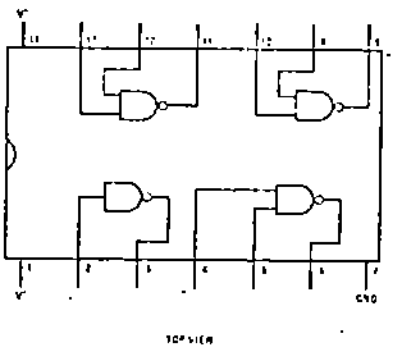
features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

schematic and connection diagrams



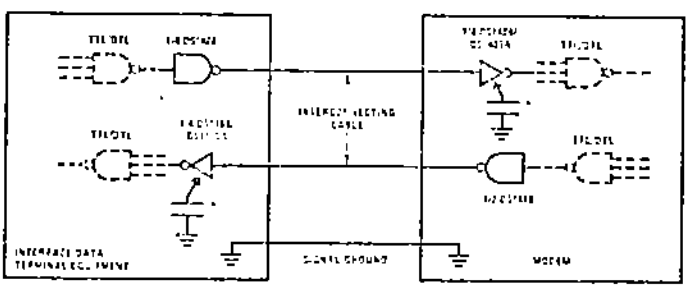
Dual-In-Line Package



Order Number DS1488J

typical applications

RS232C Data Transmission



absolute maximum ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 15.0V$			0.005	10.0	μA
V_{OH}	High Level Output Voltage	$R_L = 3.0 k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$	6.0	7.0		V
			$V^+ = 13.2V, V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0 k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$	−6.0	−6.8		V
			$V^+ = 13.2V, V^- = -13.2V$	−9.0	−10.5		V
I_{OS}^+	High Level Output Short Circuit Current	$V_{OUT} = 0V, V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{OS}^-	Low Level Output Short Circuit Current	$V_{OUT} = 0V, V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V, V_{OUT} = \pm 2V$		300			Ω
I_{CC}^+	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V, V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V, V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V, V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V, V^- = -15V$		8.0	12.0	mA
I_{CC}^-	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		13.0	−17.0	mA
			$V^+ = 12V, V^- = -12V$		−17.0	−23.0	mA
			$V^+ = 15V, V^- = -15V$		−23.0	−31.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		−0.01	−1.0	mA
			$V^+ = 12V, V^- = -12V$		−0.01	−1.0	mA
			$V^+ = 15V, V^- = -15V$		−0.01	−2.5	mA
P_D	Power Dissipation	$V^+ = 9.0V, V^- = -9.0V$			252	333	mW
		$V^+ = 12V, V^- = -12V$			414	576	mW

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pLH}	Propagation Delay to a Logical "1"	$R_L = 3.0 k\Omega, C_L = 15 pF, T_A = 25°C$		250	350	ns
t_{pHL}	Propagation Delay to a Logical "0"	$R_L = 3.0 k\Omega, C_L = 15 pF, T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0 k\Omega, C_L = 15 pF, T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0 k\Omega, C_L = 15 pF, T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1458.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

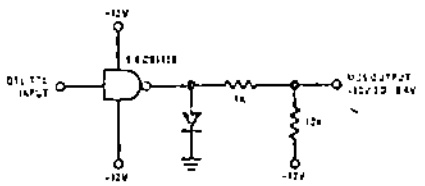
$$C = I_{SC}\,(\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

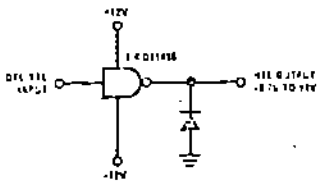
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

typical applications (con't)

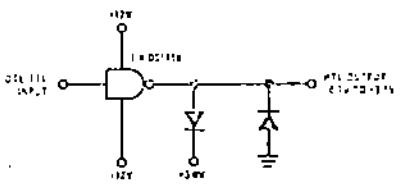
DTL/TTL-to-MOS Translator



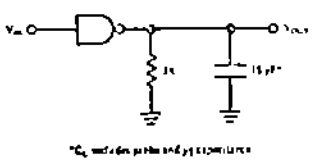
DTL/TTL-to-HTL Translator



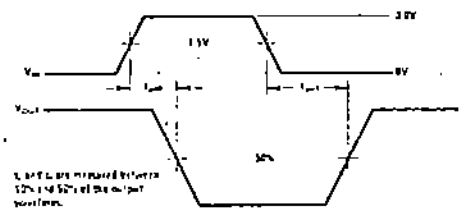
DTL/TTL-to-RTL Translator



ac load circuit

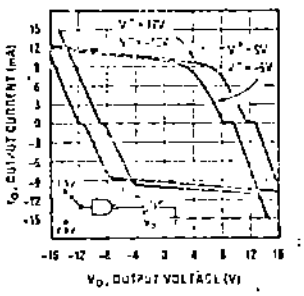


switching time waveforms



typical performance characteristics

Output Voltage and Current-Limiting Characteristics



NATIONAL

Line Drivers/Receivers

DS1489/DS1489A quad line receiver

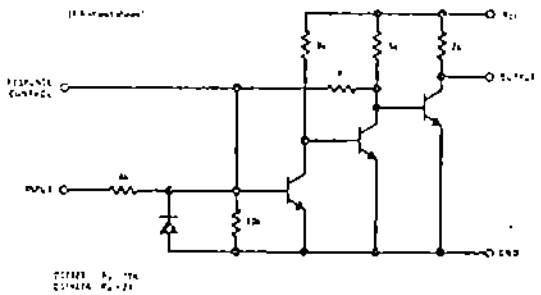
general description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The DS1489/DS1489A are available in 14-lead ceramic dual in line package.

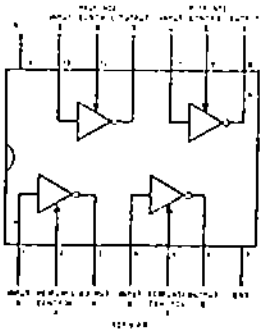
features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

schematic and connection diagrams

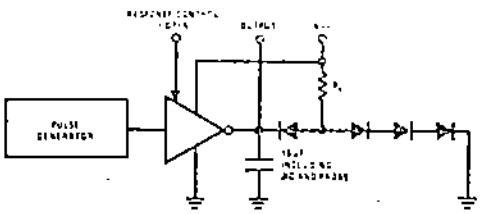


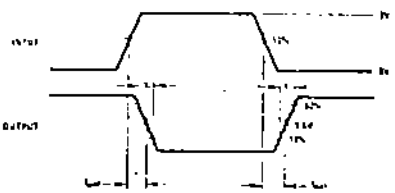
Dual In Line Package



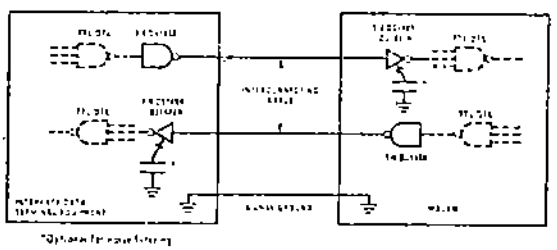
Order Number DS1489J or DS1489AJ

ac test circuit and voltage waveforms

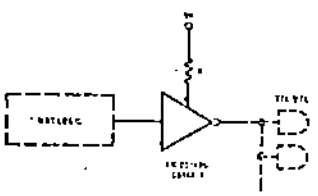




typical applications



RS232C Data Transmission



MOS to TTL/DTL Translator

absolute maximum ratings (Note 1)

The following apply for T_A = 25°C unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Input High Threshold Voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10 mA	DS1489	1.0		1.5	V
			DS1489A	1.75		2.25	V
V_{TL}	Input Low Threshold Voltage	T_A = 25°C, V_{OUT} ≥ 2.5V, I_{OUT} = −0.5 mA		0.75		1.25	V
I_{IN}	Input Current	V_{IN} = +25V		+3.6	+5.6	+8.3	mA
		V_{IN} = −25V		−3.6	−5.6	−8.3	mA
		V_{IN} = +3V		+0.33	+0.52		mA
		V_{IN} = −3V		−0.32	−0.53		mA
V_{OH}	Output High Voltage	I_{OUT} = −0.5 mA	V_{TH} = 0.75V	2.6	3.8	5.0	V
			Input = Open	2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	V_{IN} = 3.0V, I_{OUT} = 10 mA			0.32	0.45	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.75V			3.0		mA
I_{CC}	Supply Current	V_{IN} = 5.0V			14	26	mA
P_D	Power Dissipation	V_{IN} = 5.0V			70	130	mW

switching characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Input to Output "High" Propagation Delay	R_L = 3.9k, *(Figure 1)* (ac Test Circuit)		28	55	ns
t_{pd0}	Input to Output "Low" Propagation Delay	R_L = 390Ω, *(Figure 1)* (ac Test Circuit)		20	50	ns
t_r	Output Rise Time	R_L = 3.9k, *(Figure 1)* (ac Test Circuit)		110	175	ns
t_f	Output Fall Time	R_L = 390Ω, *(Figure 1)* (ac Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

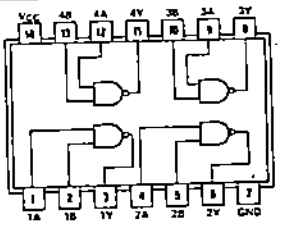
Note 4: These specifications apply for response control pin = open.

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

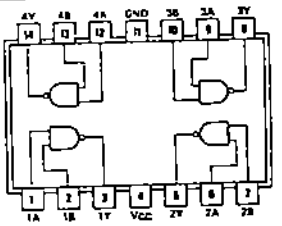
00
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 86



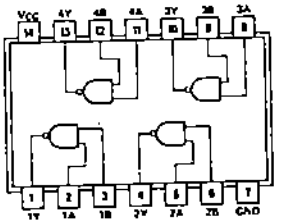
SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)



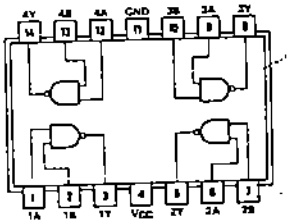
SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

01
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

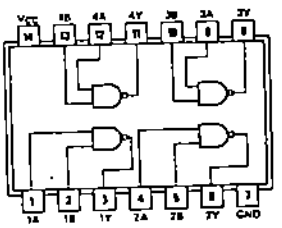
positive logic:
$Y = \overline{AB}$



SN5401/SN7401(J, N)
SN54LS01/SN74LS01(J, N, W)



SN5401/SN7401(W)
SN54H01/SN74H01(W)
SN54L01/SN74L01(T)



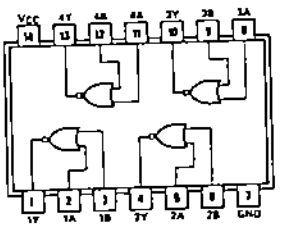
SN54H01/SN74H01(J, N)

See page 88

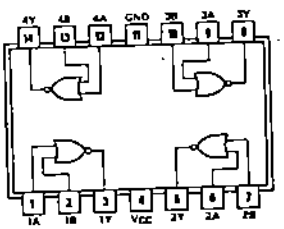
02
QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

See page 92



SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



SN5402/SN7402(W)
SN54L02/SN74L02(T)

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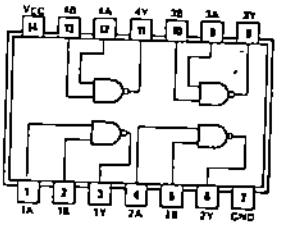
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

See page 88

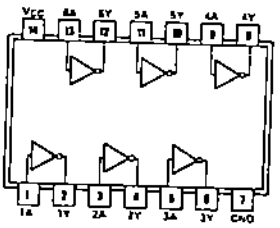


SN5403/SN7403(J, N)
SN54L03/SN74L03(J, N)
SN54LS03/SN74LS03(J, N, W)
SN54S03/SN74S03(J, N, W)

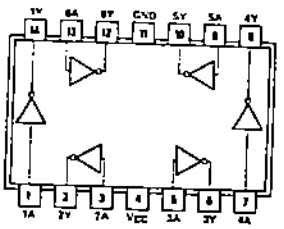
04
HEX INVERTERS

positive logic:
$Y = \overline{A}$

See page 86



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)

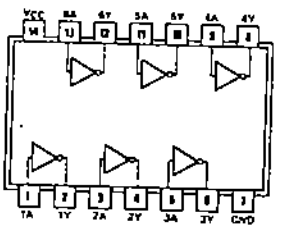


SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

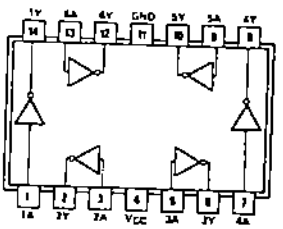
05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A}$

See page 88



SN5405/SN7405(J, N)
SN54H05/SN74H05(J, N)
SN54LS05/SN74LS05(J, N, W)
SN54S05/SN74S05(J, N, W)

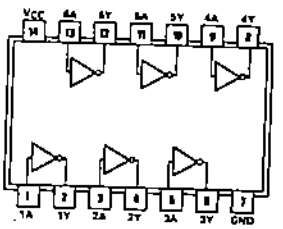


SN5405/SN7405(W)
SN54H05/SN74H05(W)

06
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106



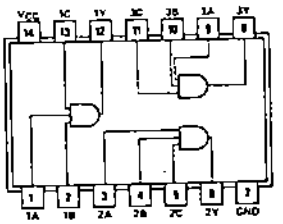
SN5406/SN7406(J, N, W)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

15
TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = ABC$

See page 96

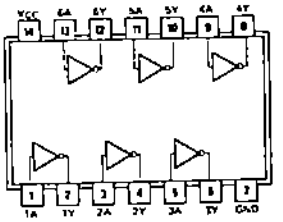


SN54H15/SN74H15(J, N, W)
SN54LS15/SN74LS15(J, N, W)
SN54S15/SN74S15(J, N, W)

16
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106

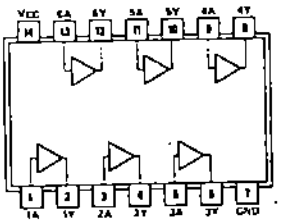


SN5416/SN7416(J, N, W)

17
HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = A$

See page 106

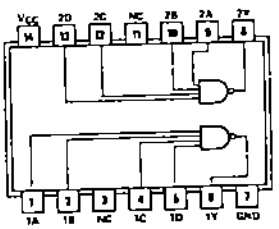


SN5417/SN7417(J, N, W)

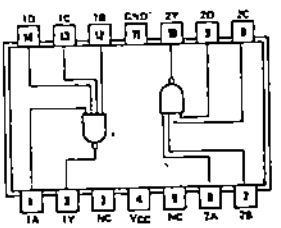
20
DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$

See page 86



SN5420/SN7420(J, N)
SN54H20/SN74H20(J, N)
SN54L20/SN74L20(J, N)
SN54LS20/SN74LS20(J, N, W)
SN54S20/SN74S20(J, N, W)



SN5420/SN7420(W)
SN54H20/SN74H20(W)
SN54L20/SN74L20(T)

NC—No internal connection

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MONOSTABLE MULTIVIBRATORS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

MONOSTABLE MULTIVIBRATORS

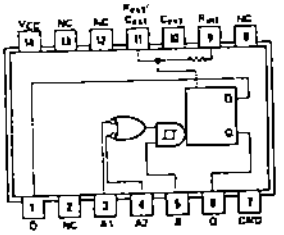
121

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊔
↓	H	H	⊓	⊔
↓	↓	H	⊓	⊔
L	X	↑	⊓	⊔
X	L	↑	⊓	⊔

See page 134

See Notes



SN54121/SN74121(J, N, W)
SN54L121/SN74L121(J, N, T)
'121 . . . R_{int} = 2 kΩ NOM
'L121 . . . R_{int} = 4 kΩ NOM

NC—No internal connection

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

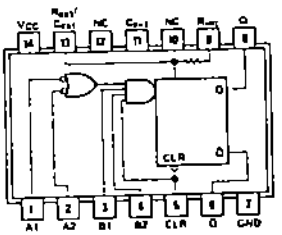
122

FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	H	H	L	H
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

See page 138

See Notes



SN54122/SN74122(J, N, W)
SN54L122/SN74L122(J, N, T)
'122 . . . R_{int} = 10 kΩ NOM
'L122 . . . R_{int} = 20 kΩ NOM

NC—No internal connection

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

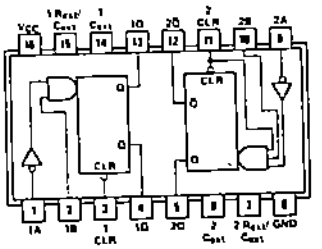
123

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

See page 138

See Notes



SN54123/SN74123(J, N, W)
SN54L123/SN74L123(J, N)

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⊓ = one high-level pulse, ⊔ = one low-level pulse, X = irrelevant (any input, including transitions).
B. To use the internal timing resistor of '121, 'L121, '122, or 'L122, connect R_{int} to V_{CC}.
C. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
D. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
E. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

TEXAS INSTRUMENTS
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125
QUADRUPLE B
WITH THREE-S
positive logic:
Y = A
Output is off (d
See page 142

126
QUADRUPLE B
WITH THREE-S
positive logic:
Y = A
Out[illegible] off (di
See page 142

128
SN54128 . . . 75-
SN74128 . . . 50-
positive logic:
Y = $\overline{A+B}$
See page 104

132
QUADRUPLE 2-I
POSITIVE-NAND
SCHMITT TRIGG
positive logic:
Y = $\overline{AB}$
See page 98

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54121/SN54L121 and 2 kΩ to 40 kΩ for the SN74121/SN74L121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_T R_T \ln 2 \approx 0.7\ C_T R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

recommended operating conditions

		54 FAMILY / 74 FAMILY	SN54121 / SN74121			SN54L121 / SN74L121			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−200	μA
Low-level output current, I_{OL}					16			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B		1			1			V/s
	Logic inputs, A1, A2		1			1			V/μs
Input pulse width, $t_{w(in)}$			50			100			ns
External timing resistance, R_{ext}		54 Family	1.4		30	1.4		30	kΩ
		74 Family	1.4		40	1.4		40	
External timing capacitance, C_{ext}			0		1000	0		1000	μF
Duty cycle	R_T = 2 kΩ				67			67	%
	R_T = MAX R_{ext}				90			90	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54121 / SN74121			SN54L121 / SN74L121			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+} Positive-going threshold voltage at A input	V_{CC} = MIN		1.4	2		1.4	2	V

Input pulse width, $t_w(in)$		54 Family	1.4	30	1.4	30	kΩ
External timing resistance, R_{ext}		74 Family	1.4	40	1.4	40	
External timing capacitance, C_{ext}			0	1000	0	1000	μF
Duty cycle	R_T = 2 kΩ			67		67	%
	R_T = MAX R_{ext}			90		90	
Operating free-air temperature, T_A		54 Family	−55	125	−55	125	°C
		74 Family	0	70	0	70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54121 SN74121			SN54L121 SN74L121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2		1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2		1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		0.8	1.35		V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			*−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	A1 or A2			40			20	μA
		V_I = 2.4 V	B			80			40	
I_{IL}	Low-level input current	V_{CC} = MAX,	A1 or A2			−1.6			−0.8	mA
		V_I = 0.4 V	B			−3.2			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX	54 Family	−20		−55	−10		−27	mA
			74 Family	−18		−55	−9		−27	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		13	25		7	12	mA
			Triggered		23	40		9	20	

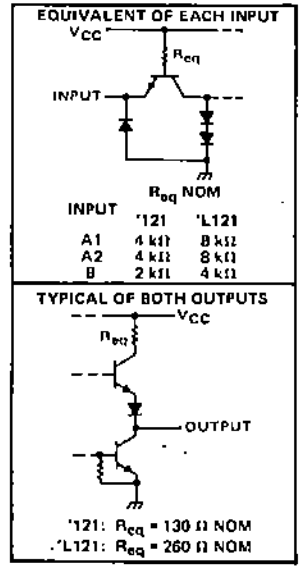
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
#Not more than one output should be shorted at a time.
*The input clamp voltage specification is effective for Series 54/74 parts date coded 7332 or higher.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'121 MIN	'121 TYP	'121 MAX	'L121 MIN	'L121 TYP	'L121 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output from either A input	C_L = 15 pF, R_L = 400 Ω for '121, R_L = 800 Ω for 'L121, See Note 1	C_T = 80 pF, R_{int} to V_{CC}	25	45	70			140	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input			15	35	55			110	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from either A input			30	50	80			160	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from B input			20	40	65			130	ns
$t_{w(out)}$	Pulse width obtained using internal timing resistor		C_T = 80 pF, R_{int} to V_{CC}	70	110	150	70	225	260	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance		C_T = 0, R_{int} to V_{CC}	20	30	50	20	35	70	ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		C_T = 100 pF, R_T = 10 kΩ	600	700	800	600	700	850	ns
			C_T = 1 μF, R_T = 10 kΩ	6	7	8	6	7	8	ms

NOTE 1: Load circuit and voltage waveforms are shown on page 148.

schematics of inputs and outputs



TYPICAL CHARACTERISTICS§

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

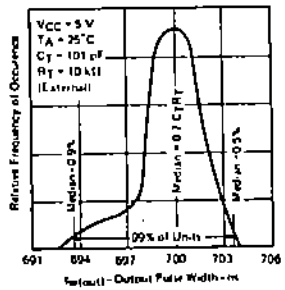


FIGURE 1

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE AIR TEMPERATURE

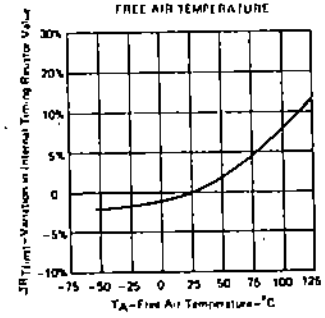


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

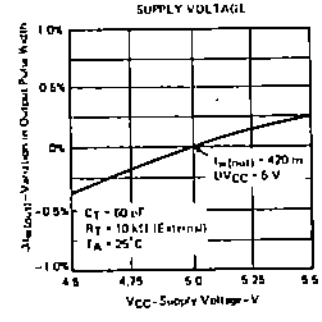


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE AIR TEMPERATURE

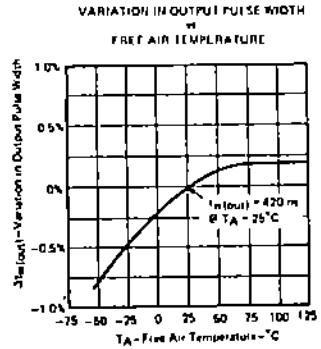


FIGURE 4

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE AIR TEMPERATURE

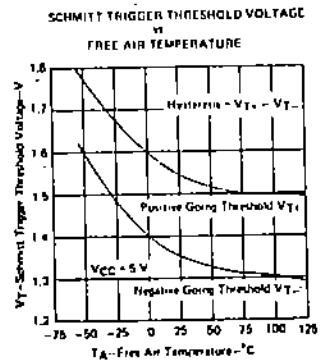


FIGURE 5

§Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121 only.

TYPICAL CHARACTERISTICS§ (continued)

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§Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121 only.

TYPICAL CHARACTERISTICS§ (continued)

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

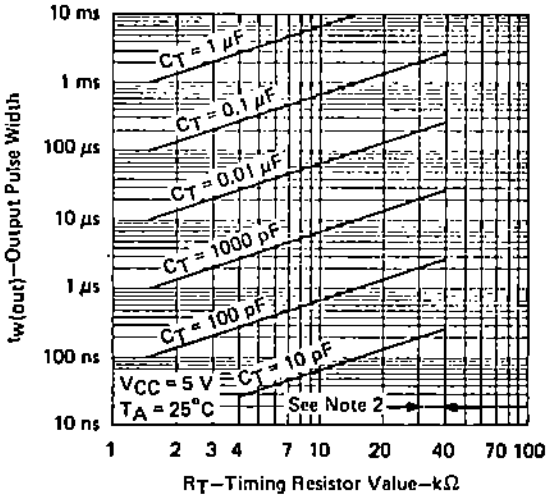


FIGURE 6

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

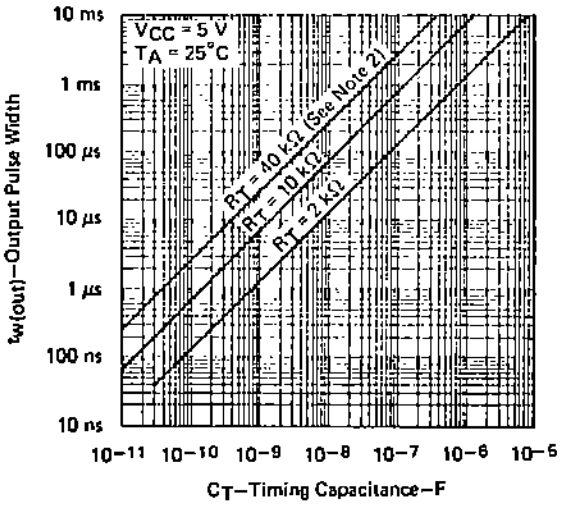
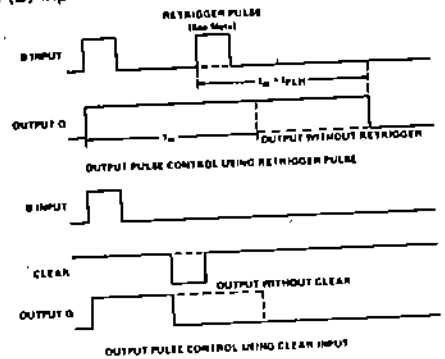


FIGURE 7

§Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121 only.
NOTE 2: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54121 and SN54L121.

description

The '122, '123, 'L122, and 'L123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

FIGURE A—TYPICAL INPUT/OUTPUT PULSES

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The '122 and 'L122 each has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with '121 or 'L121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor),
C_{ext} is in pF,
t_w is in ns,
K is 0.32 for '122, 0.28 for '123, 0.37 for 'L122, 0.33 for 'L123.

For pulse widths when $C_{ext} \leq 1000$ pF, see Figures B and C.

'122, '123
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

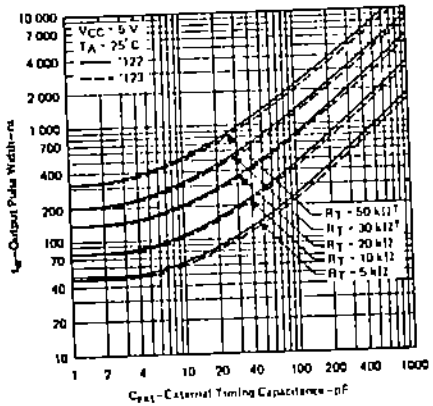


FIGURE B

'L122
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

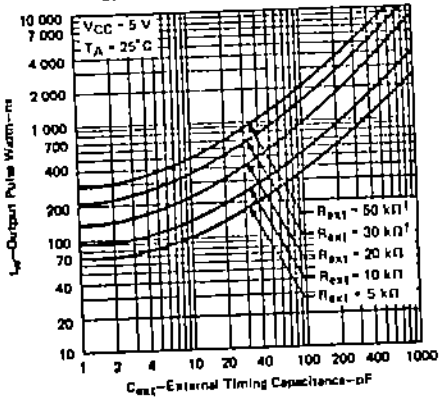


FIGURE C

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' and SN54L' circuits.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74			SERIES 54L / SERIES 74L			UNIT
		'122, '123			'L122, 'L123			
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
				−800			−400	μA

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor),
C_{ext} is in pF,
t_w is in ns,
K is 0.32 for '122, 0.28 for '123, 0.37 for 'L122, 0.33 for 'L123.

For pulse widths when $C_{ext} \leq 1000$ pF, see Figures B and C.

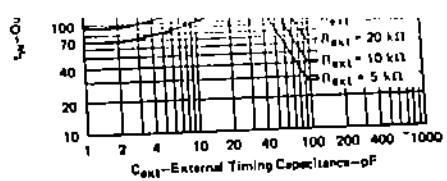


FIGURE C

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' and SN54L' circuits.

recommended operating conditions

		54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '122, '123			SERIES 54L / SERIES 74L 'L122, 'L123			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400	μA
Low-level output current, I_{OL}					16			8	mA
Pulse width, t_w	A or B inputs high		40			50			ns
	A or B inputs low		40			50			
	Clear low		40			50			
External timing resistance, R_{ext}		54 Family	5		25	5		25	kΩ
		74 Family	5		50	5		50	
External capacitance, C_{ext}			No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal					50			50	pF
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SERIES 54 / SERIES 74 '122, '123			SERIES 54L / SERIES 74L 'L122, 'L123			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, I_{OH} = MAX, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX, See Note 1		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current	Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			20	μA
	Clear input				80			40	
I_{IL} Low-level input current	Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−0.8	mA
	Clear input				−3.2			−1.6	
I_{OS} Short-circuit output current*		V_{CC} = MAX, See Note 1	−10		−40	−5		−20	mA
I_{CC} Supply current (quiescent or triggered)	'122, 'L122	V_{CC} = MAX, See Notes 2 and 3		23	28		11	14	mA
	'123, 'L123			46	66		23	33	

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
*Not more than one output should be shorted at a time.
NOTES: 1. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
2. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 or 'L122 is open.
3. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 or 'L122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 4

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	'122, '123 TEST CONDITIONS	'122, '123 MIN	'122, '123 TYP	'122, '123 MAX	'L122, 'L123 TEST CONDITIONS	'L122, 'L123 MIN	'L122, 'L123 TYP	'L122, 'L123 MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 400 Ω		22	33	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 800 Ω		44	66	ns
	B				19	28			38	56	
t_{PHL}	A	$\overline{Q}$			30	40			60	80	ns
	B				27	36			54	72	
t_{PHL}	Clear	Q			18	27			36	54	ns
t_{PLH}		$\overline{Q}$			30	40			60	80	
t_{wQ} (min)	A or B	Q			45	65			90*	130*	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω	'122			C_{ext} = 400 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 800 Ω	'L122			μs
				3.08	3.42	3.76		1.7	1.9	2.1	
				'123				'L123			
				2.76	3.03	3.37		1.5*		2.1*	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{wQ} = width of pulse at output Q
*These values for 'L123 are tentative.
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

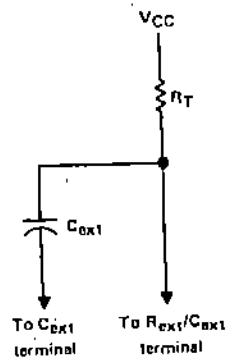
TYPICAL APPLICATION DATA

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure E be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

$$t_w = K_D \cdot R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

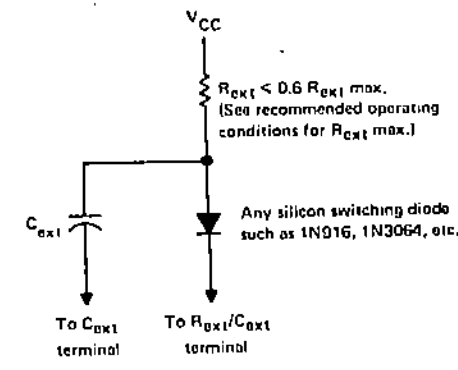
where

R_{ext} is in kΩ,
C_{ext} is in pF,
t_w is in ns,
K_D is 0.28 for '122, 0.25 for '123, 0.33 for 'L122, and 0.29 for 'L123.



TIMING COMPONENT CONNECTIONS WHEN C_{ext} < 1000 pF

FIGURE D



TIMING COMPONENT CONNECTIONS WHEN C_{ext} > 1000 pF AND CLEAR IS USED

FIGURE E

recommended operating conditions

	SN54279 MIN	SN54279 NOM	SN54279 MAX	SN74279 MIN	SN74279 NOM	SN74279 MAX	UNIT
	4.5	5	5.5	4.75	5	5.25	V

schematics of inputs and outputs

TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44, SN7442A THRU SN7444A, SN74L42 THRU SN74L44
4-LINE-TO-10-LINE DECODERS (1-OF-10)

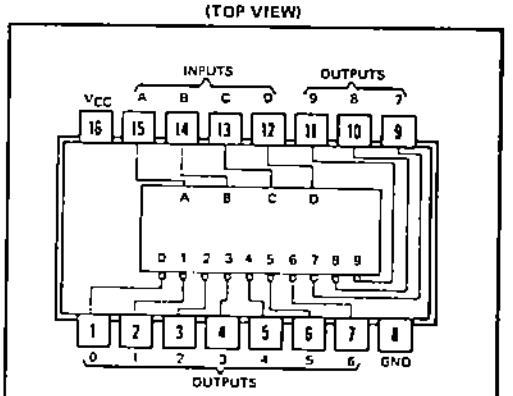
BULLETIN NO. DL-S 7211861, DECEMBER 1972

'42A, 'L42 . . . BCD-TO-DECIMAL
'43A, 'L43 . . . EXCESS-3-TO-DECIMAL
'44A, 'L44 . . . EXCESS-3-GRAY-TO-DECIMAL

- Also for Application as
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'L42, 'L43, 'L44	70 mW	49 ns

SN54'/SN74' . . . J, N, OR W PACKAGE
SN54L'/SN74L' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'L42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt.

The 'L42, 'L43, 'L44 decoders are designed specifically for power-critical or battery-operated systems. The '42A, '43A, and '44A decoders are intended for higher-performance systems especially new designs, where power is not critical. For ultra-high performance and/or speed-critical memory decoders, the SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

FUNCTION TABLE

NO.	'42A, 'L42 BCD INPUT				'43A, 'L43 EXCESS-3 INPUT				'44A, 'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

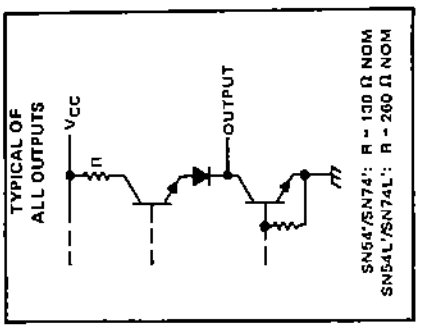
H = high level, L = low level

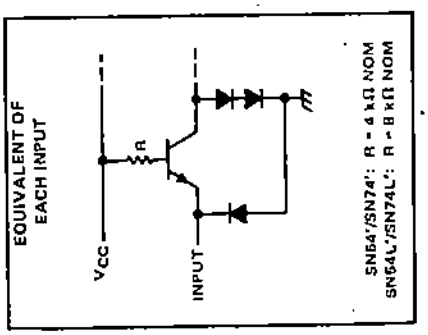
functional block diagrams and schematics of inputs and outputs

'44A, 'L44
EXCESS-3-GRAY-TO-DECIMAL DECODERS

'43A, 'L43
EXCESS-3-TO-DECIMAL DECODERS

'42A, 'L42
BCD-TO-DECIMAL DECODERS





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5442A SN5443A SN5444A			SN7442A SN7443A SN7444A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

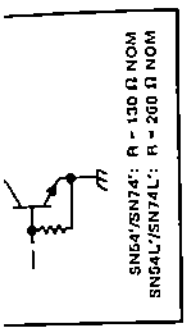
PARAMETER		TEST CONDITIONS†	SN5442A SN5443A SN5444A			SN7442A SN7443A SN7444A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		28	41		28	56	mA

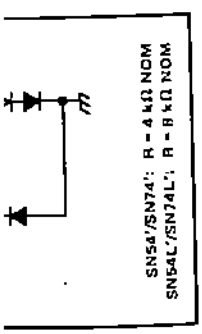
†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 3: Load circuits and waveforms are shown on page 148.





TYPES SN54L42, SN54L43, SN54L44, SN74L42, SN74L43, SN74L44
4-LINE-TO-10-LINE DECODERS (1-OF-10)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54L' Circuits . . . . . −55°C to 125°C
SN74L' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54L42, SN54L43, SN54L44			SN74L42, SN74L43, SN74L44			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 8 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−9		−28	mA
I_{CC}	Supply Current	V_{CC} = MAX, See Note 2		SN54L'		14	22	mA
				SN74L'		14	28	

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C_L = 15 pF, R_L = 800 Ω, See Note 3	10	44	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			46	70	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic		10	34	50	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			52	70	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TTL
MSI

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

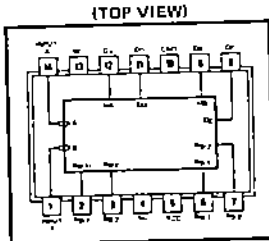
BULLETIN NO. DL-S 7211807, DECEMBER 1972

'90A, 'L90 . . . DECADE COUNTERS

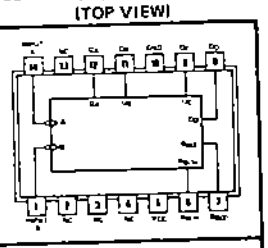
'92A . . . DIVIDE-BY-TWELVE COUNTER

'93A, 'L93 . . . 4-BIT BINARY COUNTERS

'90A . . . J, N, OR W PACKAGE
'L90 . . . J, N, OR T PACKAGE
(TOP VIEW)

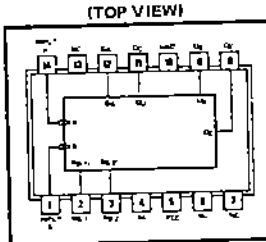


'92A . . . J, N, OR W PACKAGE
(TOP VIEW)

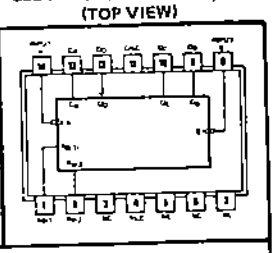


positive logic: see function tables

'93A . . . J, N, OR W PACKAGE
(TOP VIEW)



'L93 . . . J, N, OR T PACKAGE
(TOP VIEW)



positive logic: see function tables

NC—No internal connection

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'L90, divide-by-six for the '92A, and divide-by-eight for the '93A and 'L93.

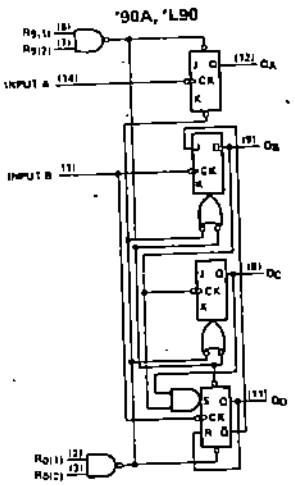
All of these counters have a gated zero reset and the '90A and 'L90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'L90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

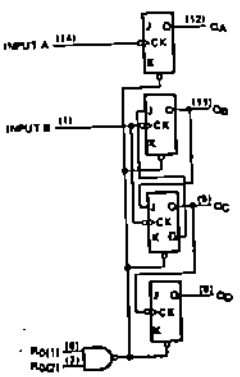
TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'92A, '93A	130 mW
'L93	16 mW

functional block diagrams

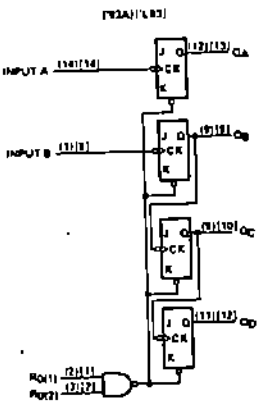
'90A, 'L90



'92A



'93A, 'L93



↓ . . . dynamic input activated by transition from a high level to a low level.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

'90A, 'L90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

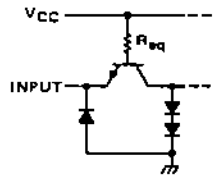
'92A, '93A, 'L93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

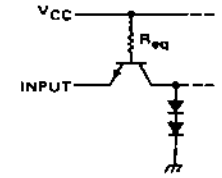
schematics of inputs and outputs

'90A, '92A, '93A
EQUIVALENT OF EACH INPUT



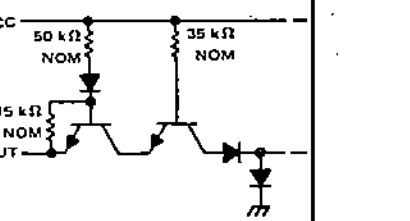
INPUT	R_{eq} NOM
A	2.5 kΩ
B ('90A, '92A)	1.25 kΩ
B ('93A)	2.5 kΩ
All resets	6 kΩ

'L90, 'L93
EQUIVALENT OF EACH INPUT EXCEPT A AND B OF 'L93

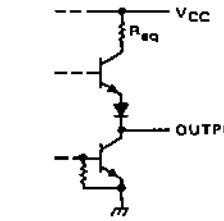


INPUT	R_{eq} NOM
A ('L90)	13.3 kΩ
B ('L90)	6.67 kΩ
All resets	40 kΩ

'L93
EQUIVALENT OF A OR B INPUT



'90A, '92A, '93A, 'L90, 'L93
TYPICAL OF ALL OUTPUTS



'90A, '92A, '93A: R = 100 Ω NOM
'L90, 'L93: R = 500 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A . . . . . −55°C to 125°C
SN7490A, SN7492A, SN7493A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN5490A, SN5492A, SN5493A			SN7490A, SN7492A, SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup, t_{setup}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'90A MIN	'90A TYP‡	'90A MAX	'92A MIN	'92A TYP‡	'92A MAX	'93A MIN	'93A TYP‡	'93A MAX	UNIT
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	Any reset	V_{CC} = MAX, V_I = 2.4 V			40			40			40	μA
		A input				80			80			80	
		B input				120			120			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6	mA
		A input				−3.2			−3.2			−3.2	
		B input				−4.8			−4.8			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	−20		−57	−20		−57	mA
			SN74'	−18		−57	−18		−57	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Figure 1	32	42		32	42		32	42		MHz
	B	Q_B		16			16			16			
t_{PLH}	A	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	A	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	B	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	B	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	24							

¶ f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 8 V
Input voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN54L90, SN54L93 Circuits . . . . . −55°C to 125°C
SN74L90, SN74L93 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 4. Voltage values are with respect to network ground terminal.
5. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L90, SN54L93			SN74L90, SN74L93			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input count frequency, f_{count}	0		3	0		3	MHz
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Width of input count pulse, $t_{w(count)}$	200			200			ns
Width of reset pulse, $t_{w(reset)}$	200			200			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'L90			'L93			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_{OH}	High-level output voltage	SN54L'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.3		V
		SN74L'		2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	SN54L'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX§		0.15	0.3		0.15	0.3	V
		SN74L'			0.2	0.4		0.2	0.4	
I_I	Input current at maximum input voltage	Any reset input	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		A input				300			200	
		B input				600			200	
I_{IH}	High-level input current	Any reset input	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		A input				30			20	
		B input				60			20	
I_{IL}	Low-level input current	Any reset input	V_{CC} = MAX, V_I = 0.3 V			−0.18			0.18	mA
		A input				−0.54			0.36	
		B input				−1.08			0.36	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		4	7.2		3.2	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
¶ Outputs are tested at I_{OL} = MAX plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'L90			'L93			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum count frequency		3	6		3	6		MHz
t_{PLH}	Propagation delay time, low-to-high-level Q_D output from input A	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		230	340		280	450	ns
t_{PHL}	Propagation delay time, high-to-low-level Q_D output from input A			230	340		280	450	ns

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